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Design and analysis of a novel quasi Z source based asymmetric multilevel inverter for PV applications

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ABSTRACT

A novel Quasi Z source (QZS) based Asymmetric Multilevel Inverter for Photovoltaic application is proposed in this paper. It consists of an Impedance source-based dc-dc converter and Asymmetric Multilevel Inverter (AMLI). QZS network can buck/boost the input DC voltage eliminating separate DC-DC boost converter. MLI topology with reduced switches and DC input provide high quality output with large levels. DC input magnitude of the inverter is based on an algorithm. The system ensures high voltage gain, low switching stress, lessened gate circuitry, high reliability and better harmonic profile. Low THD values ensures reduced filter size and hence cost. The theoretical concepts and parameter design of the proposed topology is illustrated in detail. The performance analysis is verified using Matlab/Simulink environment.

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1. INTRODUCTION

Renewable power generation has witnessed its largest ever growth with a global addition of 181 gigawatts (GW) in the year 2018, totalling the capacity to 2376GW. Solar photovoltaic (PV) installation has shown a consistent growth with an addition of 100GW accounting for 55% share amongst other renewables [1]. For renewable energy harvesting and grid integration, power electronic converters play a key role. Multilevel inverters (MLI) proves to be the best choice for Photovoltaic energy conversion systems [2-3]. Types of MLI's with control and application have been addressed in many literatures[4].They play a major role in renewable energy based modern power system applications including High Voltage Direct Current (HVDC) transmission,Flexible AC Transmission Systems (FACTS),Unified Power Flow Controllers (UPFC),Active filters,Solid State Transformers (SST) and commercial and industrial applications such as conveyors,rolling mills,mine hoists,marine propulsion,motor drives for traction,Magnetic Resonance Imaging System (MRI) etc [5-6].

MLI's synthesize multilevel output voltage from different combinations of input DC sources and switches. The N level output waveform has improved harmonic profile, high efficiency, reduced switching loss,less dv/dt stress and better electromagnetic compatibility[2, 7].Multilevel converters are mainly classified into three classic structures :Neutral Point Clamped [8],Flying Capacitor [9] and Cascaded H Bridge [10].But large number of power devices and related drive circuitry makes the system more complex at higher levels [8].Among the classical structures, Cascaded H Bridge Multilevel Inverter(CHBMLI) needs relatively small number of power electronic components to achieve more levels at output[4].CHB permits different values of input DC sources and it can be added or subtracted to get more levels at the output making

it appropriate for PV applications [2, 11].Many newer topologies including 3 level active NPC (3L-ANPC), 3 level FC,5 level H bridge NPC,NPC-CHB,Modular Multilevel Converters (MMC),P2 topology and 5 level active NPC (5L-ANPC) have made their way to industry [4].In addition,many modulation methods such as carrier based Sinusoidal Pulse Width Modulation (SPWM),Space Vector Modulation(SVM) and control strategies such as Model predictive control, Voltage Oriented Control (VOC), sliding mode control etc were developed to cater large number of MLI's [4-5]. CHBMLI's are mainly classified as symmetric and asymmetric depending on the magnitude of input DC voltage sources [12]. Symmetric topology offers high modularity. But large number of switches in the circuit results in increased cost and complexity. Asymmetric configuration needs lesser number of circuit elements, but different input DC magnitude makes its practical implementation more complex [2]. Many modified topologies for symmetric and asymmetric multilevel inverters are available in the literature [13, 14]. The DC input sources are based on binary and trinary arrangement. An algorithm is utilized to determine the dc input magnitude [14].

Voltage Source Inverter (VSI) is a buck inverter with its peak AC output lower than the DC input [15]. In a photovoltaic system, a dc-dc converter is required between PV panel and the inverter to boost the dc input to the inverter [2]. This configuration is termed as a two-stage system which reduces the efficiency and increases the complexity and cost [16-17]. Conventional boost converter is assumed to have infinite voltage gain as its duty cycle can be varied between 0 to 1. But the circuit parasitic elements restrict the voltage gain [18-19]. To mitigate the drawbacks of a two-stage system, Impedance source based single stage system was introduced [2]. The first impedance (Z) source network was introduced by F.Z. Peng [15]. The Z source concept is pertinent to any ac/dc power converters. It is a two-port network with L and C components and utilizes the shoot through state for boosting action [2, 15]. Z source inverter (ZSI) can be Voltage / Current source type [2].Based on magnetics they are broadly classified as transformer/non transformer based [20].Non transformer based topologies include Z source and Quasi Z Source topologies .Transformer coupled include Y source,Γ source,T source,TZ source,LCCT Z source,Trans Z source and HF transformer isolated Z source[20-22].Four quasi Z source inverters (qZSI) were proposed in [23] to attain constant input current and a common dc rail between the input and inverter bridge [2]. Lower passive component ratings and reduced source stress are the significant features of qZSI compared to ZSI [2, 24].

A novel QZS based Asymmetric Multilevel Inverter (AMLI) is presented in this paper. It is a single stage MLI structure for a grid connected photovoltaic system where the conventional dc-dc converter (boost) stage is eliminated [2]. It reduces the number of power conversion stages thereby improving reliability of the system [17]. QZS network with a power semiconducting switch 'M' for DC-DC power conversion was introduced in [23]. They can act as a buck/boost converter [25]. QZS network boosts the dc input to provide it to the multilevel inverter [2, 26]. It offers constant input current with high voltage gain same as that of an Z source circuit. Capacitor voltage stress is reduced compared to ZSI and shares a common ground between the input and output [27]. A simplified structure of cascaded asymmetric multilevel inverter with reduced switches and DC sources is used in the circuit [2]. The proposed structure generates more output voltage levels with reduced input sources and power semiconducting switches. Algebraic sum of all the possible combinations of DC inputs are utilised to generate required levels at the output [12]. Proposed converter generates a 31-level output with the DC input provided from a Quasi Z Source network and is validated using Matlab.

2. QZS BASED ASYMMETRIC CHB MULTI LEVEL INVERTER

Figure 1 shows the proposed AMLI structure. It is a combination of two converters: Quasi Z Source network and AMLI. The Quasi Z Source Converter (QSZC) consists of an LC network and a MOSFET 'M'. The regulated QZSC output is given as input to the inverter [2, 27]. QZSC1 and QZSC3 provide input's to AMLI represented as VA1 and VA2.Similarly the output's of QZSC2 and QZSC4 is represented as VB1 and VB2.Quasi Z Source circuit comprises of inductors, capacitors, diodes and active power switches for each input. The L_f-C_f filter smoothens the output voltage [2].

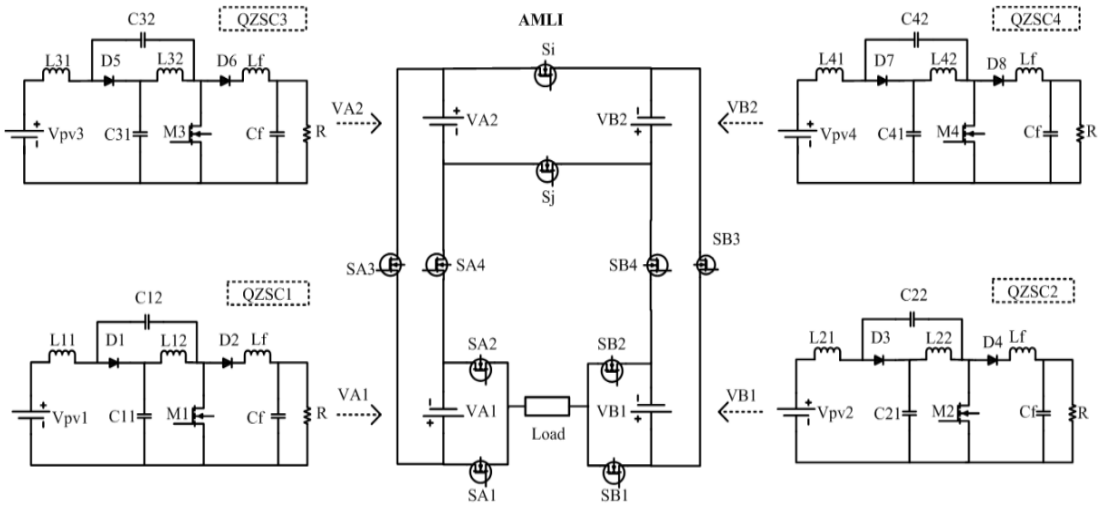

Figure 1. Proposed QZS based AMLI

The power switches and circuit elements are assumed to be ideal and the converter operates in steady state. Pulse Width Modulation (PWM) is provided for the switch M [16]. Here the first stage deals with the operation of Quasi Z Source converter (QZSC) and the next stage explains the operation of the MLI:

2.1. Analysis of quasi Z source converter

PV panel or any dc source can provide input to the Quasi Z Source network. Four QZSC networks namely $QZSC_1$, $QZSC_2$, $QZSC_3$ and $QZSC_4$ are utilized to generate required number of output voltage levels. Let V_{PV1}, V_{PV2}, V_{PV3} and V_{PV4} provides the DC input to each QZS network. Each QZSC has two operating modes viz. Mode I and Mode II [2].

2.1.1. Mode I

Consider the Quasi Z Source converter, QZSC1.During mode I, Mosfet 'M1' is ON and diode D1 is OFF. The dc input V_{PV1} and the capacitor voltage V_{C12} magnetizes the inductor L_{11}.The inductor L_{12} gets magnetized by the capacitor voltage V_{C11} [2]. The converter operates as depicted in Figure 2.

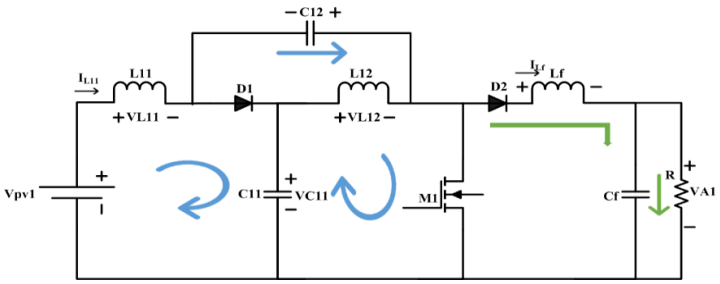

Figure 2. $QZSC_1$ operation during Mode I

2.1.2. Mode II

Figure 3 shows Mode II operation. During Mode II, Mosfet 'M' is OFF and the diode 'D1' is ON [2]. The DC input V_{PV1} and the inductor's L_{11} and L_{12} supplies energy to the resistive load R. Capacitor C_{11} is charged by V_{PV1} and L_{11} and C_{12} is charged from L_{12}. Boosted output voltage from the QZS based dc-dc converter is provided as dc link voltage to the multilevel inverter. DC link voltage balance is a tough task for a grid connected MLI.Numerous voltage control strategies are mentioned in the literature [2, 4].

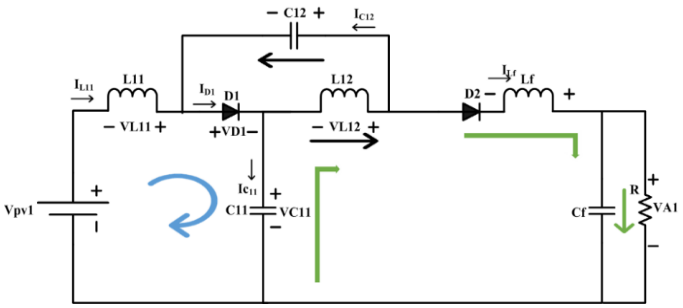

Figure 3. $QZSC_1$ operation during mode II

2.2. Analysis of AMLI

Asymmetric Multilevel Inverter (AMLI) forms the next stage of the proposed system [2]. To generate 'm' level output, conventional structure needs 2(m-1) switches. 'm' represents the levels at the output. To generate 31 level output,60 switches and 15 DC sources are required for a conventional system. This increases the size and cost of the system reducing the efficiency and reliability of the system [17]. For optimizing the performance of the circuit, a generalized 31 level MLI topology is considered here [12]. The diagram of the AMLI is presented in Figure 4.

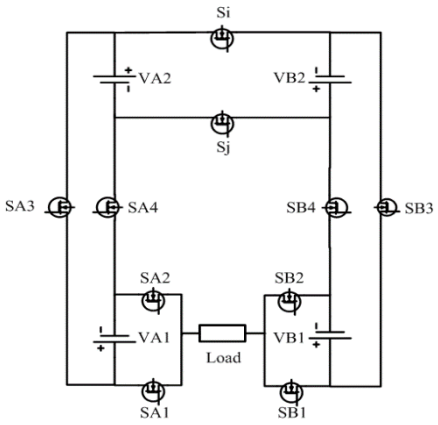

Figure 4. Circuit diagram of AMLI

H bridge consists of ten MOSFET's and four dc inputs provided from QZSC [2]. Switches in the same leg are not turned on simulataneoulsy to avoid short circuit. An algorithm decides the magnitude of the DC sources. Supply voltage polarity is a significant factor in generating required level of output voltage. Thirty-one level is obtained at the output of the inverter by different combinations of input dc [2]. In general, if 'N' represents the number of DC sources in each leg, then 2N is the total number of dc sources and 4N+2 is the total number of MOSFET's [2, 12]. Number of output voltage levels and its peak value is given by equations [2, 12],

$$N_L = 2^{2N+1} - 1 \quad (1)$$

$$V_{OM} = V_{AN} + V_{BN} \quad (2)$$

V_{OM} is the output voltage peak and V_{AN} /V_{BN} is the H Bridge input voltages.

MOSFET's used in the circuit are SA1, SA2, SA3, SA4, SB1, SB2, SB3, SB4, Si and Sj. Si and Sj should not be turned on simultaneously. Table 1 shows the switching states, DC sources utilized and the corresponding output levels. Calculation and switching states of only seven levels is presented here.

Table 1: Voltage levels and switching states of the QZSC-AMLI

Vo	SA1	SA2	SA3	SA4	SB1	SB2	SB3	SB4	Si	Sj	DC Sources used
0	0	1	0	1	0	1	0	1	0	1	0
1	1	0	0	1	0	1	0	1	0	1	VA1
2	0	1	0	1	1	0	0	1	0	1	VB1
3	1	0	0	1	1	0	0	1	0	1	VA1 + VB1
4	0	1	1	0	0	1	0	1	0	1	VA2 – VA1
5	1	0	1	0	0	1	0	1	0	1	VA2
6	0	1	1	0	1	0	0	1	0	1	VA2 + VB1 – VA1
7	1	0	1	0	1	0	0	1	0	1	VA2 + VB1

The magnitude of the DC sources of the QZS based AMLI is obtained from the expression [2] [12],

$$V_{A,K} = 5^{K-1} V_{dc} \tag{3}$$

$$V_{B,K} = 2 \times 5^{K-1} V_{dc} \text{ for K=1,2,3…n} \tag{4}$$

DC link voltage magnitude of the circuit can also be represented as [2][12],

$$V_{A1} = V_{PV1}\ , V_{B1} = 2V_{PV2}\ , V_{A2} = 5V_{PV3}\ , V_{B2} = 10V_{PV4} \tag{5}$$

3. CIRCUIT DESIGN

This section describes the design of network parameters L and C based on the operating principle explained in section 2. Consider the design of QZSC1. For a QZSC, the network parameters L_1=L_2=L and C_1=C_2=C. DT_S be the ON time of the switches (1-D) T_S be the OFF time. D denotes the duty ratio of the switch. The time integral of the inductor voltage over a complete cycle is assumed to be zero in steady state [2]. The voltage across the capacitors V_{C11} and V_{C12} can be expressed as,

$$V_{C11} = V_{PV1} \frac{(1-D)}{(1-2D)} = V_{PV1} \times B \tag{6}$$

$$V_{C12} = V_{PV1} \frac{D}{(1-2D)} = V_{PV1}(B-1) \tag{7}$$

Gain of the converter or Boost factor (B) is given by [2],

$$B = \frac{V_O}{V_{PV}} = \frac{(1-D)}{(1-2D)} \tag{8}$$

The average value of output voltage,

$$V_0 = \frac{(1-D)}{(1-2D)} \times V_{PV} \tag{9}$$

QZS provides a positive boost voltage if 0<D<0.5 and a negative voltage with 0.5<D<1 [2].
Inductor current,

$$I_{L11} = \frac{I_O(1-D)}{(1-2D)} \tag{10}$$

where $I_{L11} = I_{L12} = I_L$ and $V_{L1} = V_{L2} = V_L$
Inductance L is given by the equation below, where f_s - switching frequency in Hertz [28],

$$L = L_1 = L_2 = \frac{V_{PV}^2}{0.2 \times P_O \times f_S} \times D \times \frac{(1-D)}{(1-2D)} \quad (11)$$

Large inductor current ripple will increase stress on switch and diode. Generally, ripple is calculated using the expression [29],

$$\Delta I_L = X_L \times \%I_L \quad (12)$$

where X_L represents the allowed ripple current which ranges between 15% to 40% [2].

$$L_f \geq \frac{DR_L}{2f} \quad (13)$$

, L_f -filter inductance

Inverter's output voltage ripple and current ripple is absorbed by capacitors C_1 and C_2. The voltage ripple is assumed to be limited to 3% of the peak power [28]. Capacitance expression is given by,

$$C_1 = C_2 = \frac{2 \times P_O \times D}{0.03 \times V_{PV} \times V_{DC} \times f_S} \quad (14)$$

4. SIMULATION RESULTS

Matlab/Simulink is utilized to analyze the operating principle of the proposed topology. Let the power rating of the converter be 500Watts [2]. The magnitudes of the dc link voltages are 16V,32V,80V and 160V for V_{A1}, V_{B1}, V_{A2} and V_{B2} respectively. The switching frequency for the AMLI is taken as 20kHz with a resistive load of 100 Ω. Simulation parameters are provided in Table 2.

Table 2: Component values used for simulation

Components	$QZSC_1$	$QZSC_2$	$QZSC_3$	$QZSC_4$
L (mH)	0.0189	0.0734	0.394	1.576
C (mF)	1.38	1.031	0.2116	0.0529
V_{PV} (V)	12	12	24	24
L_f (mH)	0.0025	0.0196	0.131	0.526
C_f (mF)	1.38	1.031	0.211	0.0529

The output voltages of QZSC's are given in the Figures (5)-(8).

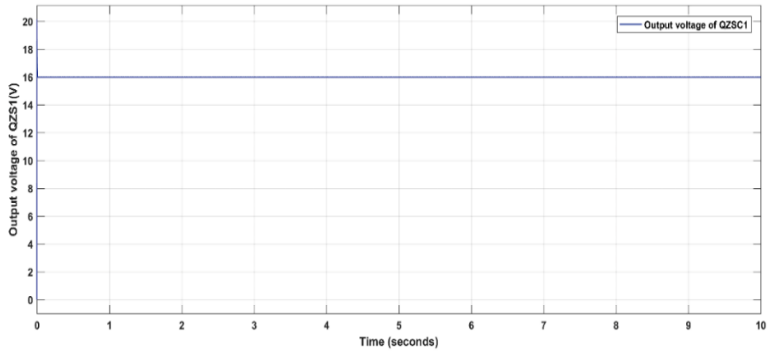

Figure 5. Output voltage of $QZSC_1$

Figure 5 shows the output voltage of $QZSC_1$.DC input V_{PV1} =12V [2]. A sample calculation of the simulation parameters for $QZSC_1$ detailed in section 3 are as follows:

Case1:
V_{PV1} = 12V, V_{A1} = 16V
From Equa. (8), Boost factor is given by the expression,

$$B = \frac{V_O}{V_{PV}} = \frac{16}{12} = 1.33 \tag{15}$$

Also $B = \frac{(1-D)}{(1-2D)}$, hence Dutyratio D = 0.198 (16)

From (11),

$$L = L_{11} = L_{12} = \frac{12^2}{0.2 \times 500 \times 20 \times 10^3} \times 0.198 \times \frac{(1-0.198)}{(1-2 \times 0.198)} = 0.0189mH \tag{17}$$

Using (14),

$$C = C_{11} = C_{12} = \frac{2 \times 500 \times 0.198}{0.03 \times 12 \times 19.86 \times 20 \times 10^3} = 1.38mF$$

The value of L_f can be calculated using (13) as follows:

$$L_f \geq \frac{DR_L}{2f} \geq \frac{0.198 \times 0.512}{2 \times 20 \times 10^3} \geq 0.0025mH \tag{18}$$

Same steps to be followed for calculating the simulation parameters for QZSC2, QZSC3 and QZSC4.

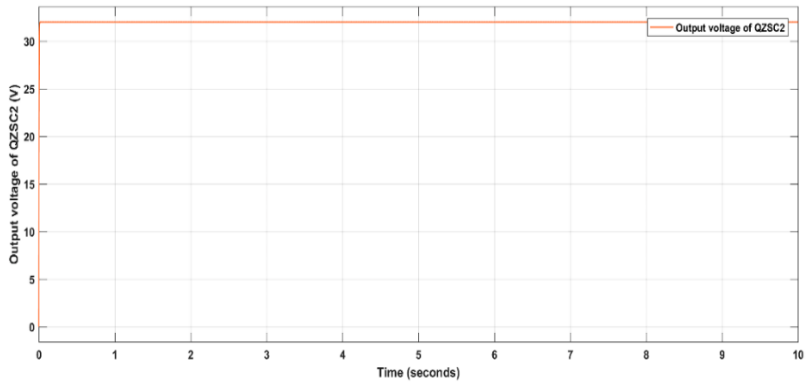

Figure 6. Output voltage of $QZSC_2$

Output waveform of $QZSC_2$ is shown in Figure 6. DC input from the PV source is V_{PV2} =12V. The dc output voltage is boosted to V_{B1}= 32V with duty ratio D=0.284. The waveform shown in Figure 7 represents the Quasi Z source converters output which acts as the DC link input to AMLI with V_{A2} = 80V with duty ratio D=0.386.

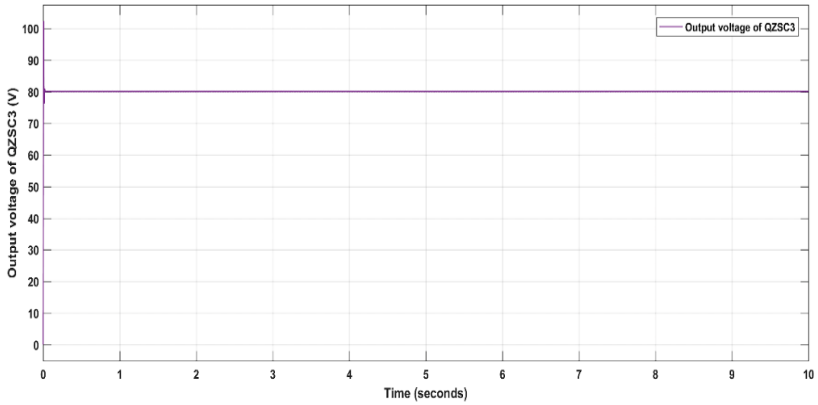

Figure 7. Output voltage of QZSC3, V_{A2}=80V with D = 0.386

Figure 8 represents the voltage output of QZSC4.It acts as input dc link voltage to the AMLI, V_{B2} = 160 V with duty ratio D=0.411.

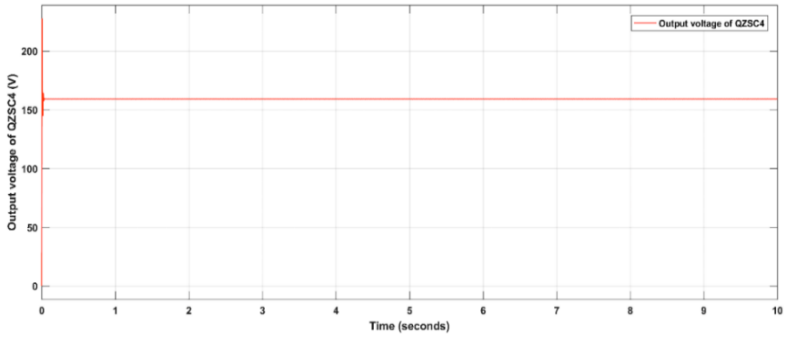

Figure 8. Output voltage of QZSC4, V_{B2}=160V with D = 0.411

MOSFET 'M' is controlled by PWM and the switching function is generated using Matlab [2]. QZSC is provided with duty ratio D1=0.198, D2=0.284, D3=0.386 and D4=0.411. MLI is fed with regulated dc output of QZSC. The output voltage of the MLI is generated by applying the switching states in proper sequence. Figure 9 represents the gate signals to the MOSFET.

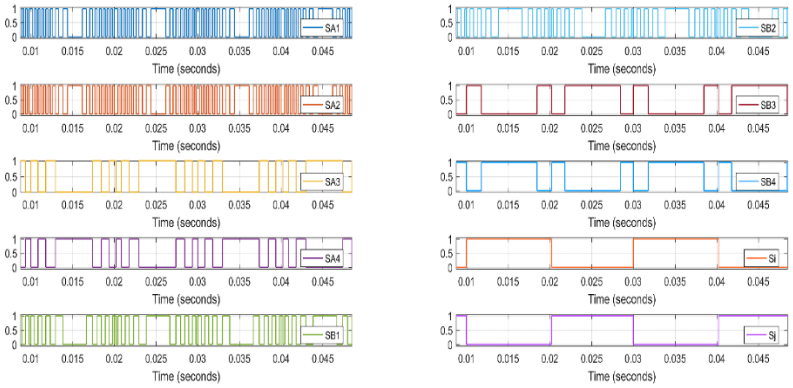

Figure 9. MOSFET switching signals

The switches are turned on in proper sequence as per the switching sequence given in Table 1. Proper care should be taken such that none of the switches in the same leg conducts together as they may destroy the switch. Figure 10 shows 31 level output of MLI.Algebraic combination of the dc inputs generate required output voltage level [2]. It generates 31levels with positive, negative and zero values [2]. The output voltage magnitude is 240V. It shows improved power quality with low THD of 2.93%. The current output shows a sinusoidal shape [2].

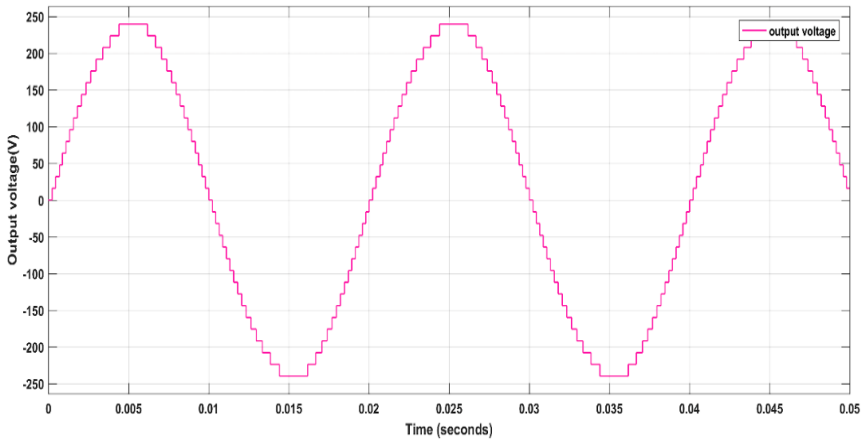

Figure 10. Output voltage of AMLI

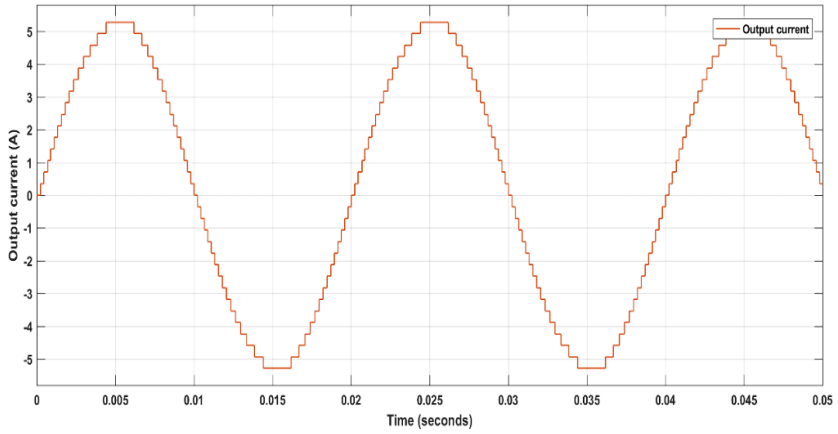

Figure 11. Load current waveform of AMLI for R load

Figure 11 shows the load current waveform with R load. The following figures represents harmonic spectrum of output voltage and current with THD_V = 2.93% and THD_I =2.9%. The waveforms are nearly sinusoidal with low THD thereby reducing filter requirements and hence cost.

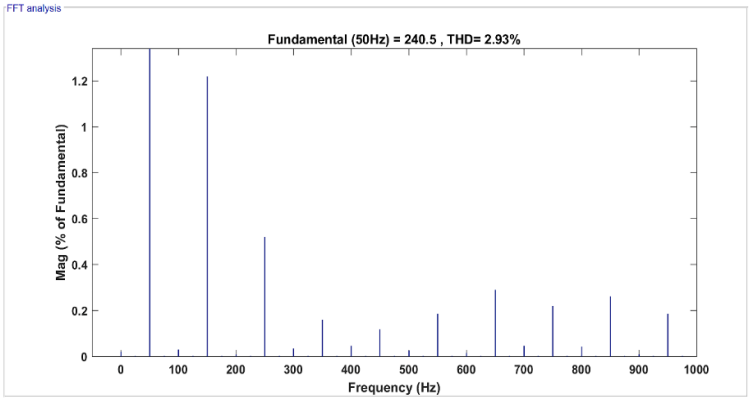

Figure 12. Output voltage Harmonic spectrum

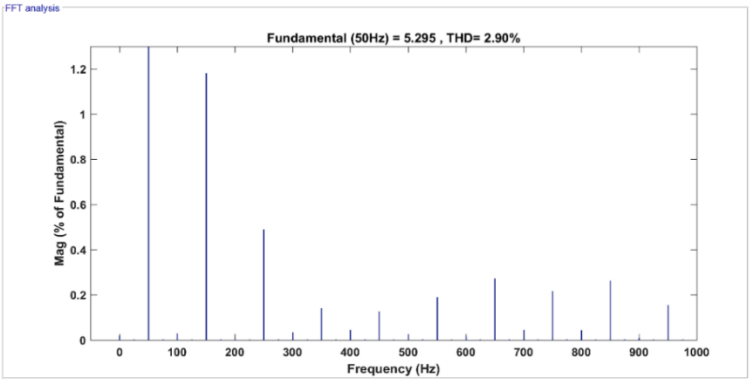

Figure 13. Output current Harmonic spectrum

5. CONCLUSION

A generalized Quasi Z Source Asymmetric Multilevel Inverter is proposed in the paper. The circuit design, analysis and simulation results are presented in detail to validate the topology. QZS network provides input DC to asymmetric 31 level inverter structure. The circuit exhibits high voltage gain and continuous input current like conventional QZSI. Large output level is achieved with reduced number of switches and input sources. It features low switching losses and reduced dv/dt stress. High quality output with low THD enables lower filter requirements. Proper DC link voltage control should be provided for the practical application of the circuit as different input sources may introduce power imbalance in the circuit. Continuous input and output currents ensures better converter performance making it suitable for Renewable energy applications.

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